What is claimed is:

Claims:

1. A semiconductor device structure comprising:

a gate electrode including a vertical sidewall and a gate dielectric covering the vertical sidewall;

at least one semiconducting carbon nanotube extending vertically between opposite first and second ends at a location adjacent to said vertical sidewall of said gate electrode;

a first contact electrically coupled with said first end of said at least one semiconducting carbon nanotube; and

a second contact electrically coupled with said second end of said at least one semiconducting carbon nanotube.

2. The semiconductor device structure of claim 1 further comprising a catalyst pad electrically coupling said conductive carbon nanotube with said gate electrode, the catalyst pad participating in the synthesis of said conductive carbon nanotube.

3. The semiconductor device structure of claim 1 wherein said at least one semiconducting carbon nanotube is a single-wall semiconducting carbon nanotube.

4. The semiconductor device structure of claim 1 further comprising:

a plurality of semiconducting carbon nanotubes extending vertically at a location adjacent to said vertical sidewall of said gate electrode.

5. The semiconductor device structure of claim 1 wherein said source includes a catalyst pad characterized by a catalyst material effective for growing said at least one semiconducting nanotube.

6. The semiconductor device structure of claim 5 wherein said first end of said at least one semiconducting carbon nanotube incorporates an electrical-conductivity enhancing substance diffused from said catalyst pad into said first end during fabrication.

7. The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said first contact and said gate electrode for electrically isolating said first contact from said gate electrode.

8. The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said second contact and said gate electrode for electrically isolating said second contact from said gate electrode.

9. The semiconductor device structure of claim 1 further comprising:

a third contact and at least one conductive carbon nanotube electrically coupling said gate electrode with said third contact.

10. The semiconductor device structure of claim 1 wherein said second contact includes a vertically-extending metal post electrically coupled with said second end of said at least one semiconducting carbon nanotube.

11. The semiconductor device structure of claim 10 wherein said second contact includes a conductive layer extending horizontally beneath said gate electrode for coupling said catalyst pad with said metal post.

12. The semiconductor device structure of claim 1 wherein said second contact includes at least one vertically-extending conductive carbon nanotube electrically coupled with said second end of said at least one semiconducting carbon nanotube.

13. The semiconductor device structure of claim 12 wherein said second contact includes a conductive layer extending horizontally beneath said gate electrode for coupling said catalyst pad with said at least one vertically-extending conductive carbon nanotube.

14. A circuit comprising an interconnected plurality of semiconductor device structures of claim 1 arranged in an array characterized by a plurality of rows and a plurality of columns.

15. The circuit of claim 14 wherein said plurality of semiconductor devices are interconnected as a memory circuit.

16. The circuit of claim 15 further comprising:

a plurality of word lines each electrically interconnecting said gate electrode of each of said plurality of semiconductor devices located in a corresponding one of said plurality of rows of said array; and

a plurality of bit lines each electrically interconnecting said second contact of each of said plurality of semiconductor devices located in a corresponding one of said plurality of columns of said array.

17. The circuit of claim 16 wherein each of said plurality of word lines comprises said gate electrode of said plurality of semiconductor devices.

18. The circuit of claim 16 wherein each of said plurality of bit lines comprises a conductive stripe electrically coupling said source of each of said plurality of semiconductor devices located in a corresponding one of said plurality of rows of said array.

19. The circuit of claim 14 further comprising:

a substrate carrying said plurality of semiconductor devices and characterized by a surface area viewed vertical to the substrate, said plurality of semiconductor devices separated by an open space that ranges from about 20 percent to about 50 percent of said surface area.

20. The circuit of claim 14 wherein said plurality of semiconductor devices are interconnected as a logic circuit.

21. A method for fabricating a circuit including an array of semiconductor device structures, comprising:

forming a stacked structure including a conducting layer, a plurality of first catalyst pads each coupled electrically with the conductive layer, a gate electrode layer, and an insulating layer separating the gate electrode layer from the plurality of first catalyst pads;

partitioning the stacked structure to define a plurality of gate electrodes in the gate electrode layer to define the array in which adjacent gate electrodes are separated by a reactant path and each of the plurality of first catalyst pads is at least partially exposed to the reactant path at a location proximate a vertical sidewall of a corresponding one of the plurality of gate electrodes; and

directing a reactant by the reactant path to each of the plurality of first catalyst pads for synthesizing at least one semiconducting carbon nanotube on each of the plurality of first catalyst pads from the reactant by a chemical vapor deposition process.

22. The method of claim 21 further comprising:

forming a plurality of second catalyst pads on the gate electrode; and

synthesizing at least one conducting carbon nanotube on each of the plurality of second catalyst pads.

23. The method of claim 21 further comprising:

defining an active area of each of the plurality of first catalyst pads.

24. The method of claim 23 wherein defining the active area further comprises:

covering a first portion of each of the plurality of first catalyst pads with a mask; and

etching a second portion of each of the plurality of first catalyst pads selective to the mask such that the first portion defines the active area.

25. The method of claim 24 wherein the mask is a temporary spacer that is removed from the device structure after etching.

26. The method of claim 21 further comprising:

forming a plurality of first contacts each electrically coupled with a first end of the at least one semiconducting carbon nanotube synthesized on a corresponding one of said plurality of first catalyst pads.

27. The method of claim 26 wherein the array is characterized by semiconductor device structures arranged in a plurality of rows and a plurality of columns, and the method further comprises:

patterning the conducting layer to define a plurality of bit lines each electrically interconnecting the first contact of all semiconductor devices located in each of the plurality of rows of the array.

28. The method of claim 27 wherein the array is characterized by semiconductor device structures arranged in a plurality of rows and a plurality of columns, and each of the plurality of gate electrodes defines a word line for the plurality of semiconductor devices located in a corresponding one of the plurality of columns of the array.

29. The method of claim 26 further comprising:

forming a plurality of second contacts each electrically coupled with a second end of the at least one semiconducting carbon nanotube synthesized on a corresponding one of the plurality of first catalyst pads.

30. The method of claim 29 further comprising:

electrically interconnecting the plurality of gate electrodes, the plurality of first contacts, and the plurality of second contacts as a logic circuit.

31. The method of claim 29 further comprising:

electrically interconnecting the plurality of gate electrodes, the plurality of first contacts, and the plurality of second contacts as a memory circuit.

32. The method of claim 21 further comprising:

diffusing an electrical-conductivity enhancing substance from each of the first plurality of catalyst pads into an adjacent end of the at least one semiconducting carbon nanotubes thereon.

33. The method of claim 32 wherein diffusing the electrical-conductivity enhancing substance occurs after directing the reactant by the reactant path to each of the plurality of first catalyst pads.